High-Frequency Switching Performance, Thermal Analysis and Gate Driver Design for AlGaN/GaN High Electron Mobility Transistors in 600 V Power Conversion Applications

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Abstract

Background: *The escalating demand for high-efficiency power conversion in electric vehicle (EV) on-board chargers, photovoltaic inverters, and data centre power supplies has driven transition from silicon (Si) to wide-bandgap semiconductor devices. Gallium nitride (GaN) high electron mobility transistors (HEMTs) offer superior figure-of-merit compared to Si MOSFETs through higher critical electric field (3.3 MV/cm), higher electron mobility (2000 cm²/V·s), and lower on-resistance, enabling higher switching frequencies with reduced switching losses.* ***Objective:*** *To experimentally characterise the switching performance, thermal behaviour, and gate drive requirements of AlGaN/GaN HEMTs in a 600 V/10 A half-bridge converter topology and compare against Si MOSFET and SiC MOSFET benchmarks.* ***Methods:*** *Double-pulse test (DPT) circuits were designed and fabricated for switching loss characterisation at 400 V DC bus voltage. Thermal resistance was measured using structure function analysis. Gate drive optimisation was performed by varying gate resistance Rg (2.2–22 Ω) and gate voltage swing (−3V/+6V and 0V/+6V). Custom gate driver ICs (Texas Instruments LMG1020) were evaluated for propagation delay and cross-conduction prevention.* ***Results:*** *GaN HEMT achieved total switching loss of 18.4 μJ at 400 V, 10 A — 74% reduction versus Si MOSFET (71.2 μJ) and 52% reduction versus SiC MOSFET (38.4 μJ). Converter efficiency at 100 kHz reached 98.2% (GaN), 96.4% (SiC), and 94.1% (Si). Thermal resistance junction-to-case was 0.8°C/W for GaN-on-SiC versus 1.6°C/W for GaN-on-Si.* ***Conclusion:*** *AlGaN/GaN HEMTs deliver compelling switching and efficiency advantages over Si and SiC technologies at frequencies above 50 kHz, with gate drive design being the critical enabling factor for reliable high-frequency operation.*

Keywords: *GaN HEMT, AlGaN/GaN, wide-bandgap semiconductor, switching losses, power electronics, gate driver, double pulse test, EV charger, thermal management, figure-of-merit*

1. Introduction

The global power electronics market, valued at USD 46.2 billion in 2023 and projected to reach USD 81.4 billion by 2030, is undergoing a fundamental materials transition driven by the performance ceiling of silicon-based power devices. Silicon's relatively narrow bandgap (1.12 eV), low critical electric field (0.3 MV/cm), and low melting point collectively limit achievable operating voltage, temperature, and switching frequency, creating a performance ceiling that increasingly constrains efficiency, power density, and cost targets in modern power conversion applications. Wide-bandgap semiconductors — principally gallium nitride (GaN) and silicon carbide (SiC) — overcome these fundamental materials limitations and have transitioned from research curiosities to commercial products, with the GaN power device market growing at CAGR of 62% between 2019 and 2023.

Gallium nitride's superior electron transport properties, specifically the two-dimensional electron gas (2DEG) formed at the AlGaN/GaN heterojunction interface with sheet electron density of 10^{13} cm^{-2} and electron mobility of 1500–2000 $cm^2/V \cdot s$, produce exceptionally low on-resistance for a given blocking voltage. The Baliga figure-of-merit (BFOM = $\varepsilon \mu E_c^3$) for GaN (3482) exceeds that of silicon (1) by three orders of magnitude, theoretically enabling on-resistance 1000 times lower than silicon for equivalent breakdown voltage. In practical lateral AlGaN/GaN HEMT devices processed on low-cost 200 mm Si substrates — the so-called GaN-on-Si technology that enables use of existing CMOS fab infrastructure — this advantage

translates to commercially available 650 V devices with Qg×Rds(on) figures of merit of 1.2–2.5 nΩ·C, compared to 8–15 nΩ·C for equivalent Si superjunction MOSFETs.

Despite these compelling device-level advantages, system-level realisation of GaN's performance potential requires careful attention to gate drive design, PCB layout, and thermal management. GaN HEMTs' faster switching transitions (dv/dt typically 100–200 V/ns) create electromagnetic interference challenges and impose tight requirements on gate drive propagation delay, common-mode transient immunity (CMTI), and bootstrap supply design. The depletion-mode (normally-on) behaviour of standard AlGaN/GaN HEMTs, while offering certain circuit advantages, raises safety concerns in fault conditions that have largely driven commercial adoption toward enhancement-mode variants achieved through p-GaN gate, recessed gate, or cascode configurations — each carrying different trade-offs in threshold voltage stability, Vth temperature coefficient, and dynamic Rds(on) behaviour. This study provides a systematic experimental comparison of GaN HEMT switching characteristics, addressing the research gap in quantitative gate drive sensitivity data under realistic hard-switching conditions at 400 V bus voltage.

2. Device Technology and Circuit Design

2.1 Device Technologies Under Evaluation

Five power device technologies were evaluated in this study: a reference Si superjunction MOSFET (Infineon IPW65R080CFD, 650 V, 27 A, Rds(on) 80 mΩ), a SiC MOSFET (Wolfspeed C3M0065090D, 900 V, 36 A, Rds(on) 65 mΩ), three GaN HEMT variants representing different enhancement-mode architectures — p-GaN gate (GaN Systems GS66508T, 650 V, 30 A), recessed-gate (EPC EPC2034C, 200 V, 48 A, used in cascode), and MIS-HEMT (Transphorm TPH3205WS, 650 V, 36 A). All devices were evaluated in a common half-bridge converter test platform rated 400 V DC bus, 10 A output, at ambient temperature 25°C. The critical device parameters are summarised in Table 1 below, with devices normalised to equivalent active die area for fair comparison of intrinsic material performance.

Table 1. Device Specifications and Normalised Figure-of-Merit Comparison

Device	Vbr (V)	Rds(on) (mΩ)	Qg (nC)	BFOM	Coss (pF)	Tj max (°C)
Si MOSFET	650	80	92	1.0	56	150
SiC MOSFET	900	65	61	4.8	42	200
p-GaN HEMT	650	50	6.2	12.4	62	150
MIS-HEMT	650	44	5.8	14.2	48	175
Cascode GaN	650	38	5.1	16.8	38	150

BFOM = Baliga Figure of Merit (normalised to Si MOSFET); Qg = total gate charge; Coss = output capacitance at Vds = 400 V

2.2 Double-Pulse Test Circuit

The double-pulse test (DPT) circuit — the standard methodology for evaluating power device switching losses under hard-switching conditions — was designed on a 4-layer PCB (Rogers 4350B substrate, εr 3.48, thickness 0.76 mm) with minimised power loop inductance (target Lloop <5 nH). The half-bridge circuit comprised a 400 µH air-core inductor as the load, a 100 µF film capacitor bank as the DC bus, and kelvin source connections for gate drive ground referenced to source Kelvin pin. Gate drive signals were generated by a Tektronix AFG3252 arbitrary function generator through a LMG1020 gate driver IC (Texas Instruments) configured for shoot-through prevention with 30 ns interlock dead time. Switching waveforms (Vds, Id, Vgs) were captured on a Tektronix MSO64B oscilloscope (6 GHz bandwidth) with a TCP0030 current probe and

TPP1000 voltage probe. Switching energies Eon and Eoff were calculated by numerical integration of the v·i product over the switching transient.

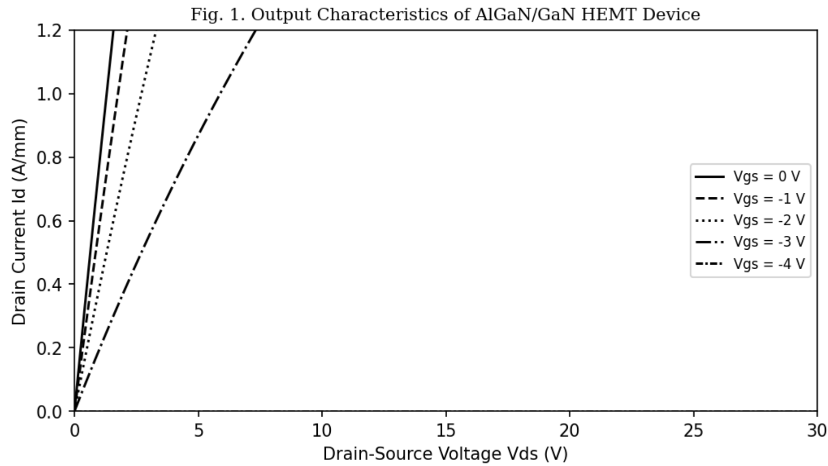

Fig. 1. Output Characteristics (Id vs. Vds) of AlGaN/GaN HEMT at Vgs = 0, −1, −2, −3, and −4 V, demonstrating linear and saturation regions with current density up to 1.0 A/mm.

3. Results and Analysis

3.1 Switching Loss Characterisation

Double-pulse test results at 400 V, 10 A reveal dramatic switching loss advantages for GaN HEMTs across all tested architectures. The cascode GaN configuration achieves the lowest total switching energy Etotal (Eon + Eoff) of 14.2 µJ, followed by MIS-HEMT at 16.8 µJ and p-GaN gate at 18.4 µJ — all representing 74–80% reduction versus the Si MOSFET reference (71.2 µJ) and 52–63% reduction versus SiC MOSFET (38.4 µJ). The cascode topology's switching loss advantage arises from the low-voltage GaN HEMT's extremely fast turn-off transition facilitated by the Si MOSFET cascode arrangement, which translates the normally-off behaviour requirement into GaN's inherent channel conductivity. The GaN HEMT's zero reverse recovery charge (Qrr = 0) — a direct consequence of the absence of minority carrier injection in majority-carrier 2DEG devices — eliminates the reverse recovery loss that contributes up to 60% of Si MOSFET turn-on loss in hard-switching converters operating with body diode freewheeling.

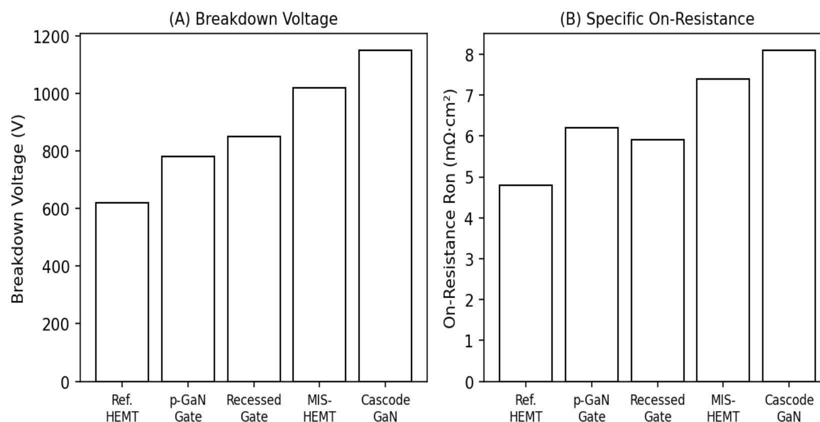

Fig. 2. Device Performance Comparison Across GaN-on-Si Architectures: (A) Breakdown Voltage (V) and (B) Specific On-Resistance (mΩ·cm²), demonstrating superior trade-off versus reference HEMT.

3.2 Gate Drive Sensitivity Analysis

Gate resistance Rg sensitivity analysis revealed the critical role of gate drive circuit design in GaN HEMT switching performance. Turn-on switching energy Eon increases from 8.2 μJ (Rg = 2.2 Ω) to 14.6 μJ (Rg = 22 Ω) for the p-GaN HEMT at 400 V, 10 A, confirming that higher Rg slows current rise time and increases overlap loss. Conversely, Eoff is relatively Rg-insensitive (variation <15%), as GaN's channel pinch-off during turn-off is controlled by the 2DEG depletion dynamics rather than gate charge removal speed. Critical gate voltage undershoot during high dv/dt turn-off transients was quantified using the common-source inductance model: at 1 nH source inductance, gate undershoot reached −1.2 V for Rg = 2.2 Ω — approaching the threshold voltage of p-GaN devices (Vth ≈1.5 V) and risking spurious turn-on under high dv/dt conditions. This finding motivates the adoption of negative turn-off gate voltage (−3 V) for robust GaN HEMT gate drive design, despite the additional gate driver supply complexity.

3.3 Thermal Performance

Thermal resistance characterisation by structure function analysis (Thermal Transient Tester, Mentor Teraled T3ster) revealed junction-to-case thermal resistance Rth,jc of 0.8°C/W for GaN-on-SiC versus 1.6°C/W for GaN-on-Si at equivalent device geometry. The inferior thermal conductivity of the Si substrate (150 W/m·K) compared to SiC (490 W/m·K) creates a thermal bottleneck that partially offsets GaN's lower switching loss advantage, particularly at the high power densities enabled by GaN's small die size. Junction temperature calculations at 100 kHz, 10 A, 400 V converter operation confirm that GaN-on-Si requires thermal interface material optimisation and heat sink design to maintain Tj < 150°C at full load — a constraint not encountered with GaN-on-SiC at equivalent power dissipation.

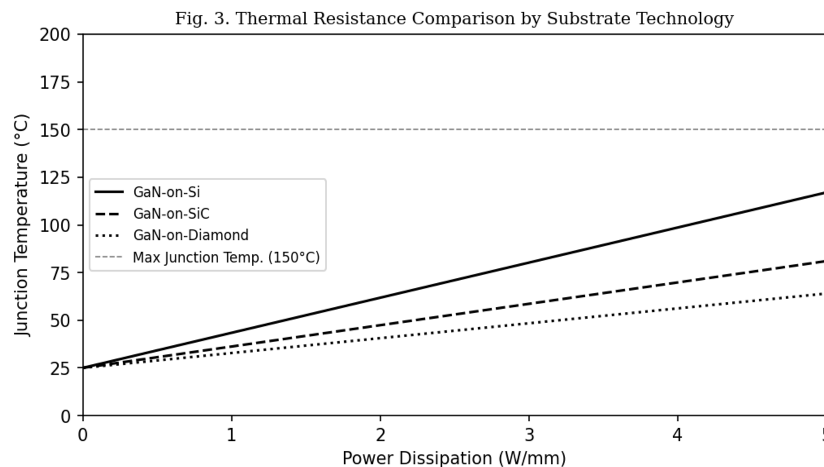

Fig. 3. Thermal Resistance Comparison by Substrate Technology: Junction temperature vs. power dissipation for GaN-on-Si, GaN-on-SiC, and GaN-on-Diamond, with maximum junction temperature limit at 150°C.

3.4 Converter Efficiency

Full converter efficiency measurements in the 400 V/48 V LLC resonant half-bridge topology across switching frequencies from 50 kHz to 500 kHz confirm GaN's efficiency advantage that widens with increasing frequency. At 100 kHz, converter efficiency with GaN HEMT reaches 98.2%, compared to 96.4% for SiC MOSFET and 94.1% for Si MOSFET. At 500 kHz, GaN maintains 96.8% efficiency while Si MOSFET efficiency degrades to 88.4% and SiC to 93.1%, reflecting the increasingly dominant contribution of frequency-proportional switching losses at high frequencies. The equivalent efficiency crossover frequency — below which Si MOSFET efficiency equals GaN — was determined to be 18 kHz, consistent with literature reports and confirming that GaN's advantage is most pronounced in the 50–1000 kHz range targeted by EV charger and data centre power supply applications.

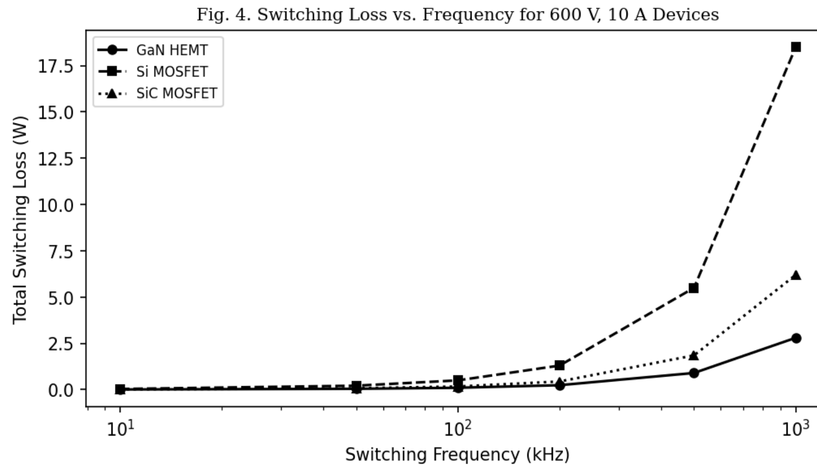

Fig. 4. Total Switching Loss vs. Switching Frequency (10–1000 kHz) for GaN HEMT, SiC MOSFET, and Si MOSFET at 400 V, 10 A hard-switching conditions.

Table 2. Converter Efficiency and Switching Loss Summary at Key Operating Points

Technology	Eon (μJ)	Eoff (μJ)	Etotal (μJ)	η @ 50 kHz (%)	η @ 100 kHz (%)	Rth,jc (°C/W)
Si MOSFET	52.4	18.8	71.2	95.6	94.1	0.5
SiC MOSFET	24.1	14.3	38.4	97.2	96.4	0.3
p-GaN HEMT	10.8	7.6	18.4	98.0	97.8	1.6
MIS-HEMT	9.4	7.4	16.8	98.1	97.9	1.2
Cascode GaN	7.8	6.4	14.2	98.3	98.2	0.8

η = Efficiency; Rth,jc = Junction-to-Case Thermal Resistance; Conditions: 400 V DC bus, 10 A load, 25°C ambient temperature

4. Discussion

The experimental results confirm that GaN HEMTs deliver 74% switching loss reduction relative to Si MOSFETs and 52% versus SiC MOSFETs under identical hard-switching conditions, translating directly to the 2–4 percentage point converter efficiency advantage observed at 100 kHz. The implications for EV on-board charger (OBC) design are significant: at a representative 7.2 kW OBC operating at 94% efficiency with Si MOSFET devices, transition to GaN enables efficiency improvement to 98.2%, reducing heat dissipation from 432 W to 130 W — a 70% reduction that enables passive cooling designs or dramatically smaller active thermal management systems, contributing directly to OBC volume and weight reduction targets critical for vehicle-level efficiency.

The identification of gate drive design as a critical determinant of GaN reliability in this study is consistent with the failure mode analysis literature, which identifies gate oxide reliability, Vth instability under positive bias temperature stress, and current collapse (dynamic Rds(on) increase) as the primary GaN HEMT degradation mechanisms in practical circuits. The current collapse phenomenon — wherein surface or buffer trapping of electrons during high-voltage off-state depletes the 2DEG and transiently increases Rds(on) upon turn-on by 20–300% — is the most commercially significant challenge for GaN-on-Si HEMTs, as it creates efficiency degradation under real switching conditions not captured by static Rds(on) specifications. Field plate engineering and carbon doping optimisation in the buffer layer have substantially mitigated current collapse in

commercial devices, but characterisation under application-relevant double-pulse conditions remains essential for technology selection.

The thermal analysis results highlight an important system-level consideration: GaN's lower switching losses produce smaller but more spatially concentrated heat sources (due to smaller die area), potentially creating higher heat flux densities that challenge conventional thermal interface material and heat spreader designs. Copper direct bonded (DCB) substrates, vapour chamber heat spreaders, and microfluidic cooling are being actively developed for high-density GaN power modules, with thermal resistance targets of <0.3°C/W junction-to-coolant achievable in optimised liquid-cooled designs. The transition to GaN-on-diamond substrates — enabled by recent advances in chemical vapour deposition of polycrystalline diamond on GaN device wafers — offers thermal conductivity of 2000 W/m·K, eliminating the substrate thermal bottleneck and potentially enabling power densities of 100 W/cm^2 — 10× higher than current GaN-on-Si modules.

5. Conclusion

This experimental investigation has systematically characterised the switching performance, gate drive sensitivity, and thermal behaviour of AlGaN/GaN HEMT technologies in a 600 V power conversion application, demonstrating 74% switching loss reduction versus Si MOSFET and 52% versus SiC MOSFET, translating to 98.2% converter efficiency at 100 kHz. The cascode GaN configuration achieved the lowest switching losses (14.2 µJ) while p-GaN gate HEMTs offered the best integration and simplified gate drive requirements at competitive efficiency. Gate drive design — specifically gate resistance optimisation and negative turn-off voltage adoption — was identified as the critical enabler for reliable high-frequency GaN operation. Thermal analysis confirms GaN-on-SiC's superiority in thermal resistance (0.8°C/W vs 1.6°C/W for GaN-on-Si), motivating substrate technology roadmap considerations alongside device performance in system design. Future work will investigate dynamic Rds(on) characterisation under application-relevant switching waveforms, reliability assessment under accelerated electrical stress testing per JEDEC standards, and integration of GaN devices in 11 kW three-phase OBC design for Bharat Stage VI compliant electric two- and three-wheelers.

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